



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

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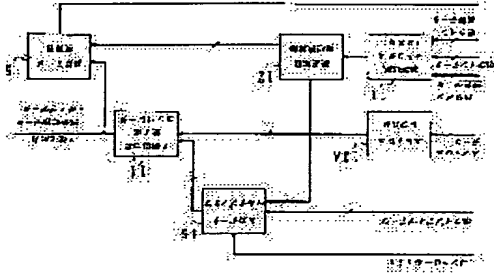
H04N 1/40
G06F 15/68

(21)Application number: 05017308 (71)Applicant: RICOH CO LTD
(22)Date of filing: 04.02.1993 (72)Inventor: KOJIMA HIDEYUKI

(54) IMAGE PROCESSOR

(57)Abstract:

PURPOSE: To provide the image processor which suppresses the increase of a space and cost at a minimum by sharing a common circuit part in the case of integrating an image processing part based on a dither method and an image processing part based on an error dispersing method or a binary error dispersion processing part and a multilevel error dispersion processing part in the same processor. CONSTITUTION: This image processor enables binary error dispersion processing and dither processing by providing a dither data input means and an input data multiplexer 16 for dither data and error dispersion processing data at a quantizing comparator 14 for binary output in a binary error dispersion processing circuit. Otherwise, this image processor enables binary error processing by and multilevel error dispersion processing by providing the quantizing comparator for multilevel

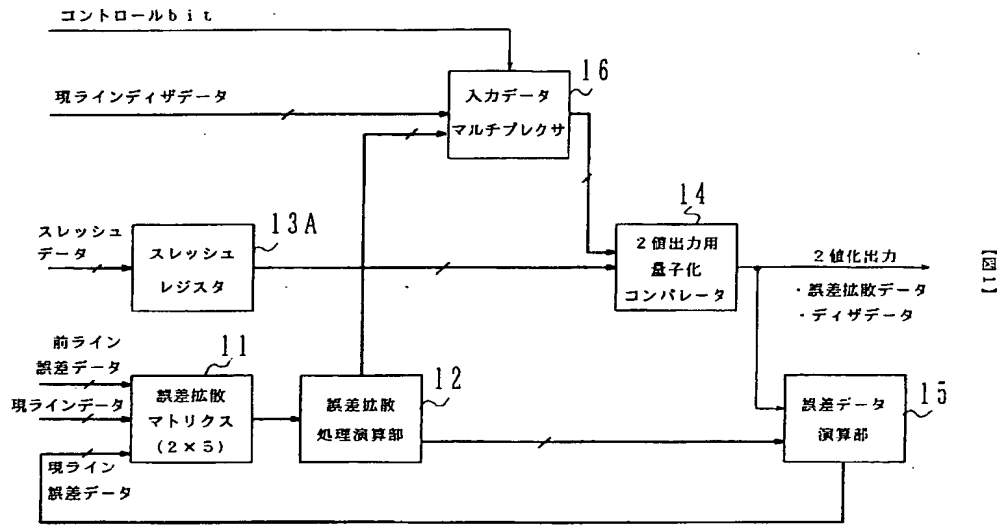


output and an encode means for this quantizing comparator output for multilevel output in addition to the quantizing comparator for binary output of a binary error diffusion processing arithmetic part 12.

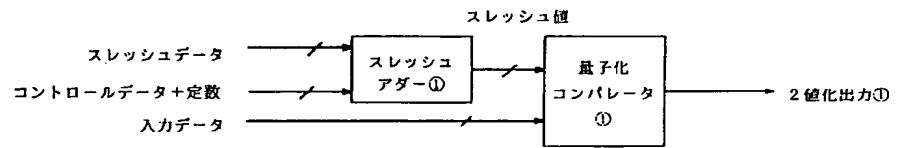
LEGAL STATUS

[Date of request for examination]
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
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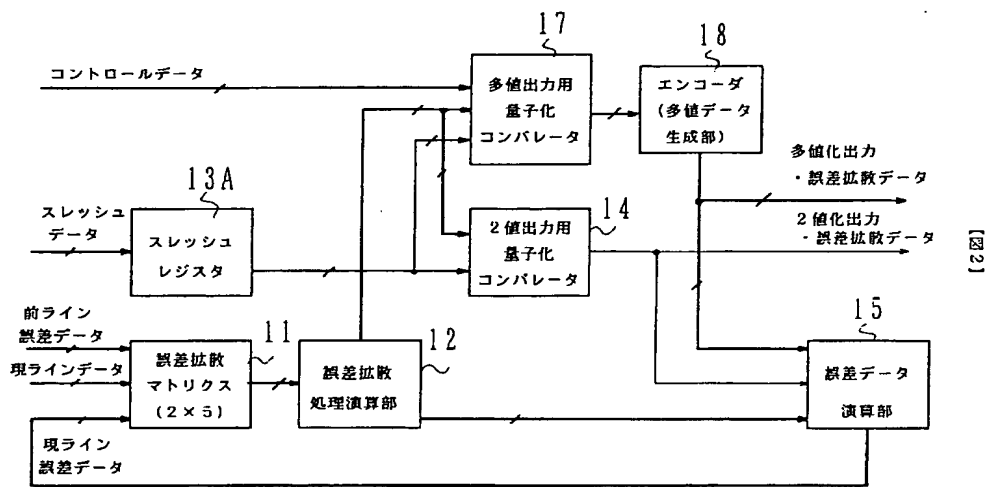


【図1】



【図5】

* n階調なら (n-1) 個分の同上スレッシュ値比較回路



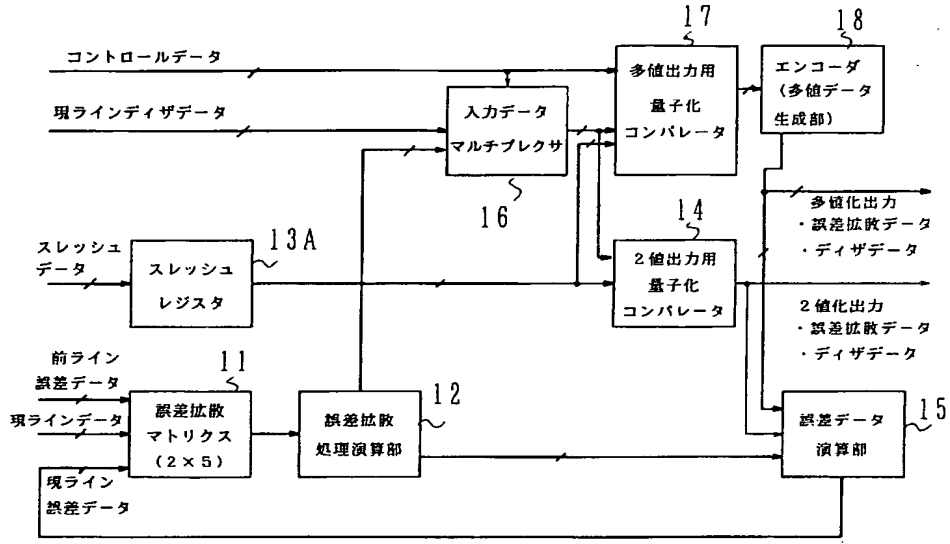
【図2】

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特開平6-233122

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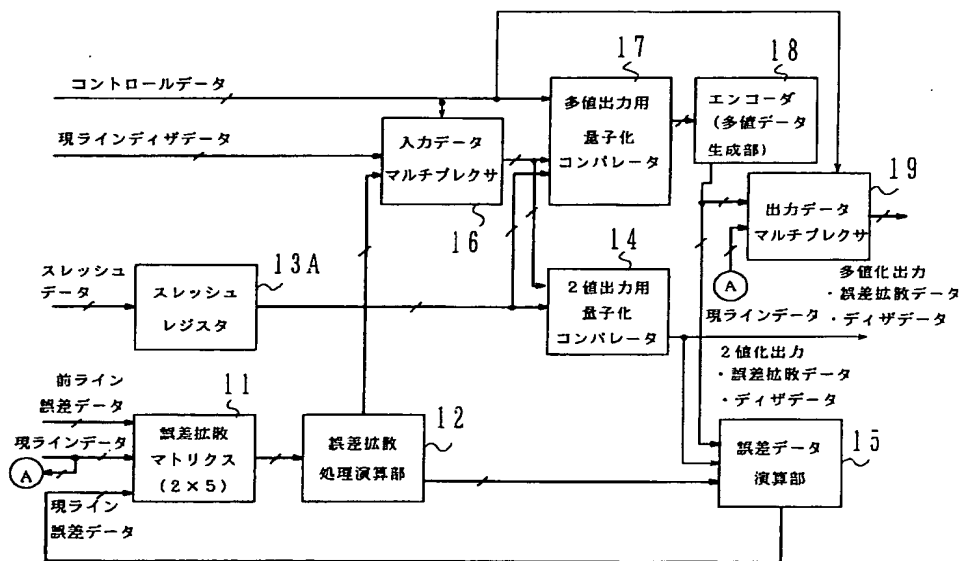
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【図3】

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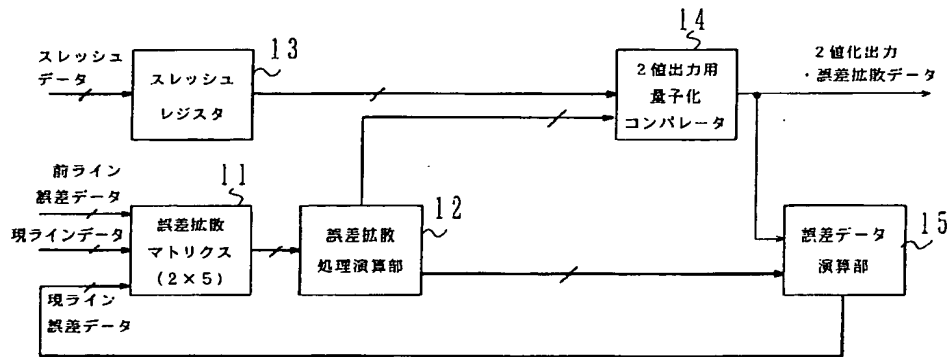
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【図4】

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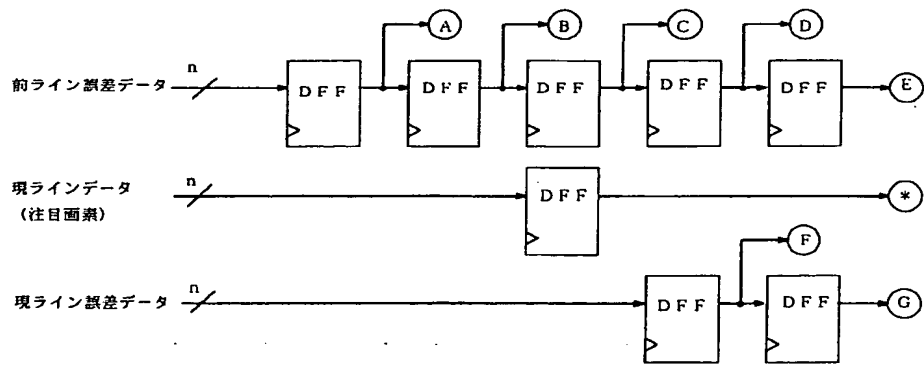
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【図6】

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特開平6-233122



【図8】

(10)

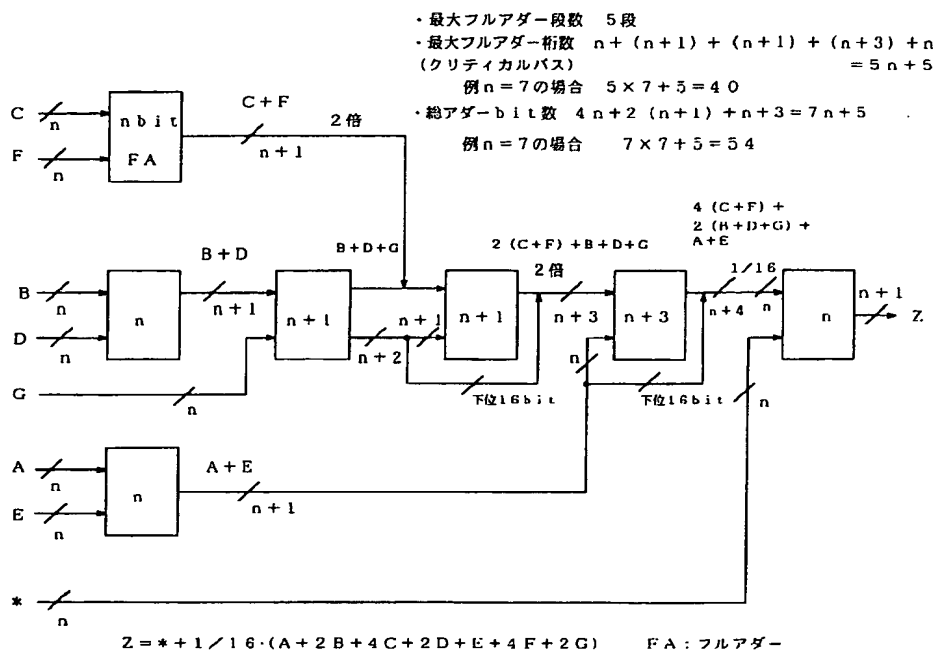
	後画素 ← 先画素				
前ライン	A	B	C	D	E
現ライン			*	F	G

重み付け係数				
1/16	2/16	4/16	2/16	1/16
		1	4/16	2/16

A~G: 誤差, *: 現 (注目) 画素, Z: 演算結果

$$Z = * + 1/16 \cdot (A + 2B + 4C + 2D + E + 4F + 2G) \dots \dots \dots (1)$$

特開平6-233122



【図9】

(11)

特開平6-233122

3 bit の2進数に変換

Y_n: コンパレータの出力
 0: データ ≤ スレッシユ
 1: データ > スレッシユ

Y₇ Y₆ Y₅ Y₄ Y₃ Y₂ Y₁
 0 0 1 1 1 1 1
 b₂ b₁ b₀
 1 0 1

【図10】

(12)

特開平6-233122